



Southern Illinois University System

Applications

- Radiation-hardened electronics
- Space satellite circuitry
- Nuclear materials and facility detection, monitoring, and operation equipment

Inventor(s)

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Dr. Watkins is a postdoctoral researcher at Los Alamos National Lab. He earned his PhD in 2016 from SIU Carbondale's department of electrical and computer engineering.

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A Highly Robust Double Node Upset Tolerant Latch

Radiation-induced or "soft" errors occur in electronic circuits when energetic particles (radiation) trigger current and voltage responses from transistors that are nominally "off." As electrical circuit components become ever smaller, circuits are increasingly susceptible to double-node upsets (DNU), during which a single radiation particle affects multiple transistors. Several solutions exist to harden circuits against DNUs, but existing designs feature performance tradeoffs, high power consumption, and long processing delays.

Invention

SIU researchers have developed an electrical latch that offers state-of-the-art performance while significantly decreasing power requirements and processing delays. Extensive HSPICE simulation has shown the device to be robust to every possible DNU error combination.

Key Advantages

- Robust performance suitable for clock gating
- Fewer transistors and failure modes as compared to state-of-the-art DNU-tolerant latches
- Lower power requirements than state-of-the-art DNU-tolerant latches
- 4x shorter processing delays as compared with state-of-the-art DNU-tolerant latches
- No performance or area tradeoff with conventional DNU-tolerant latches

Status

A provisional patent (application No. 62/394,786) was filed for this technology in September 2016. The technology is available for license.

Other opportunities related to this technology, included but not limited to sponsored and/or collaborative research, may be available. Please reach out to the designated contact identified at left for more information.